AN L-BAND TEMPERATURE COMPENSATED ULTRA LOW POWER SUCCESSIVE DETECTION LOGARITHMIC AMPLIFIER

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ABSTRACT

This paper describes a temperature compensated L-band GaAs MMIC successive detection logarithmic amplifier (SDLA) featuring ultra low power consumption. Log-linearity of ±2.5dB and a dynamic range of 60 dB was achieved over a 100 degree temperature range. This device shows no sacrifice of performance over larger, labor intensive hybrid MIC approaches.

INTRODUCTION

Logarithmic amplifiers are used to compress the dynamic range of signals so that they can be processed by devices with limited dynamic range. A type of logarithmic amplifier known as a successive detection logarithmic amplifier (SDLA) can be used to compress the dynamic range of amplitude modulated signals when the wave form of interest is the envelope. An SDLA generates a video signal which is the log of the envelope of the carrier.

Considerable advances in MMIC-based logarithmic amplifier development have been demonstrated (2, 3) despite limitations such as high power consumption or limited dynamic range based on projected channelized receiver requirements.

This paper presents a monolithic GaAs SDLA, boasting exceptionally low power consumption (700mw) with a detected log video linearity of ±2.5dB over a 100°C temperature range. The frequency range of the amplifier extends from 500 MHz to 1.2GHz.

An extensive theoretical analysis of an SDLA is given in (1). A brief overview is given below.

Figure 1 shows a block diagram of a successive detection log amplifier. The SDLA consists of several identical linear RF amplifiers in cascade. The output of each amplifier feeds a detector followed by a limiter. The logarithm of the envelope of the input RF carrier is formed at the output of the SDLA by summing the outputs of the limiters. The resulting transfer function of the SDLA is a piecewise linear approximation of a log curve as shown in Figure 2. The minimum useful input signal of the SDLA is proportional to the gain of the cascade of the RF amplifiers. The maximum useful input signal is inversely proportional to the gain of an individual amplifier stage. Thus, to achieve a large dynamic range, a large number of gain stages, with low gain per stage, is required.

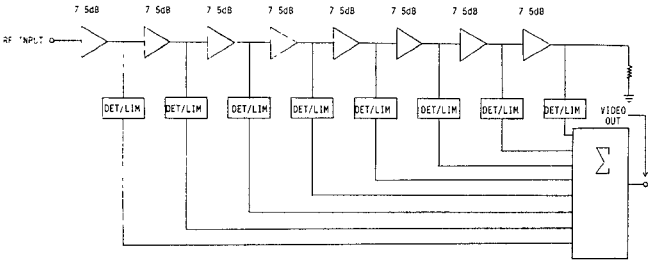

Figure 1. SDLA Block Diagram

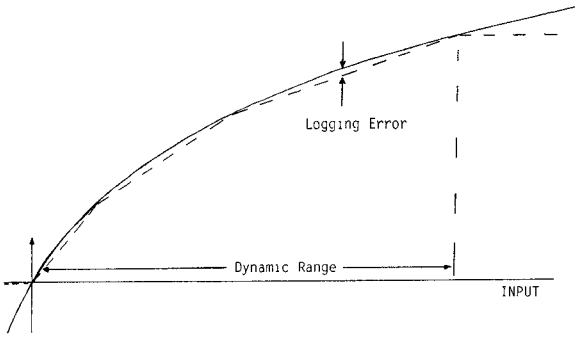

Figure 2. Piecewise Linear Approximation of a log Curve

The successive detection logarithmic amplifier topology is ideally suited for monolithic integration. This can best be appreciated by considering the practical limitations involved in fabricating an SDLA. To achieve the theoretical accuracy inherent in the piecewise linear approximation of the SDLA, all the RF amplifiers, detectors and limiters must be identical. To achieve a temperature-stable design, the sensitivity of the detectors and the limiting voltage of the limiters must not change with temperature. Fortunately, monolithic integration provides a natural way to achieve both.

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Amplifiers fabricated on the same IC chip will have nearly identical characteristics without the need for the kind of "tweaking" required in hybrids. Also monolithic integration guarantees that all components are at the same temperature. This makes it possible to use the temperature coefficient of the detector to cancel the temperature coefficient of the limiter. In a hybrid design this might not be possible because it would be difficult to guarantee that the characteristics of all the active devices would track each other with changes in temperature, partly because each device could change to a different temperature.

LOGARITHMIC AMPLIFIER DESIGN

The target specifications for the logarithmic amplifier are given below:

FREQUENCY RANGE:	750MHz to 1.5GHz
DYNAMIC RANGE:	60dB
ACCURACY:	$\pm$2.5dB (-25°C to 75°C)
POWER:	.5W

The design of an SDLA starts by determining the minimum number of stages required to meet the dynamic range and accuracy specifications. Computer simulations showed that six 10dB-amplifier stages were the minimum number required to meet the specifications. When Monte Carlo simulations were performed of a $\pm$5% gain variation between stages on the logging accuracy, it was found that an eight stage, 7.5dB per stage amplifier would be required. The simulations showed that the lower the gain per stage, the less effect on the logging accuracy from amplifier gain mismatch. Thus, an eight stage approach if preferable to the six stage approach, in spite of the added power consumption and increased complexity.

Figure 3a and Figure 3b show results of Monte Carlo simulations of a six stage and eight stage SDLA, respectively. The worst case unit-to-unit variation for the six stage unit is 2.8dB as compared with 2.5dB variation in the eight stage case.

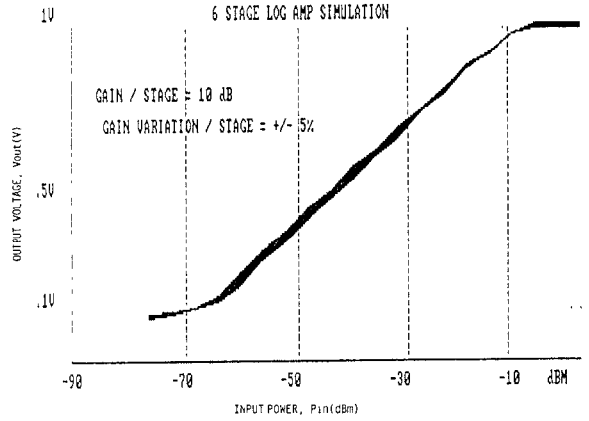

Figure 3a. Monte Carlo Simulation of 6-Stage SDLA

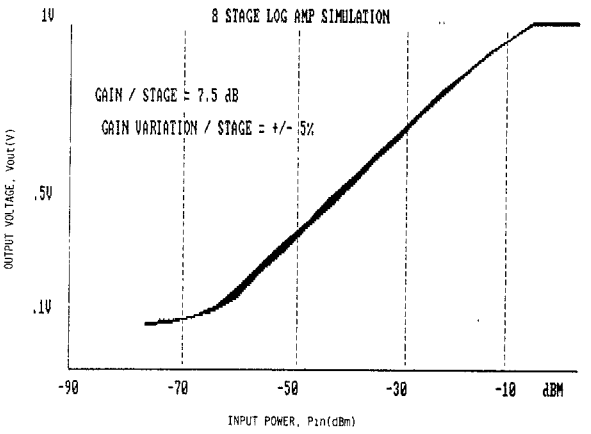

Figure 3b. Monte Carlo Simulation of 8 Stage SDLA

The severe power constraints imposed on the SDLA required that special attention be paid to the design of low power amplifiers. To conserve power, the eight RF amplifiers were designed for 150 ohm input and output impedances. Conventional 50 ohm amplifiers would draw more current. Moreover, computer simulations showed that amplifiers with an impedance higher than 150 ohms would not have sufficient bandwidth. At this impedance level, the RF amplifiers dissipated only 60mw.

The schematic of the RF amplifier is shown in Figure 4. The resistor provides feedback to stabilize the quiescent point of Q1; its value also sets the input impedance of the amplifier. The gate voltage of Q1 is set solely by the ratio of the width of Q1 to Q2 and is nearly independent of the drops in diode voltage. As a result, the gate voltage of Q1 is independent of temperature. The gate voltage of Q1 was chosen to set the quiescent current of Q1 at 1/2 I_{DSS}. At this bias point, the gain of the amplifier is nearly independent of temperature.

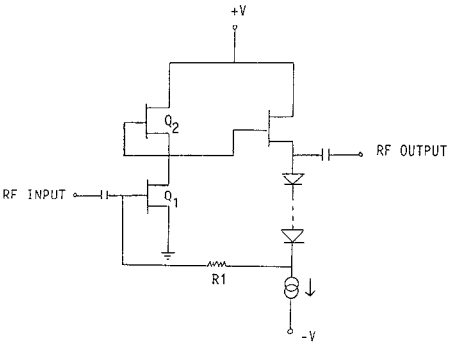

Figure 4. RF Amplifier Used in SDLA

The detector/limiter circuit was designed to peak detect with precision RF voltages from .07 to .4 volts. Driving voltages above .4 volts result in a limited output voltage of 100mv. The measured detector/limiter transfer curve at three temperatures, -25°, 25° and 80°C, appears in Figure 5. With no RF present, a small DC offset (5mv) was measured over this temperature range.

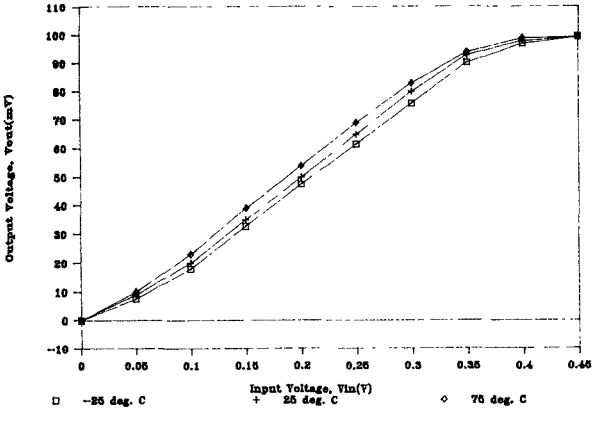

Figure 5. Measured Detector/Limiter Transfer Curve at -25°C, 25°C and 75°C

PERFORMANCE CHARACTERISTICS

Excellent linearity over changes in temperature is demonstrated in Figure 6. Here, the CW transfer curve is shown at -25°, 25° and 80°C, at a RF frequency of 1 GHz. Logging error at -25°C, 25°C and 75°C is plotted in Figure 7. Logging error is defined as any deviation from the ideal or true log curve. Maximum deviation at any point is within ±2.5dB.

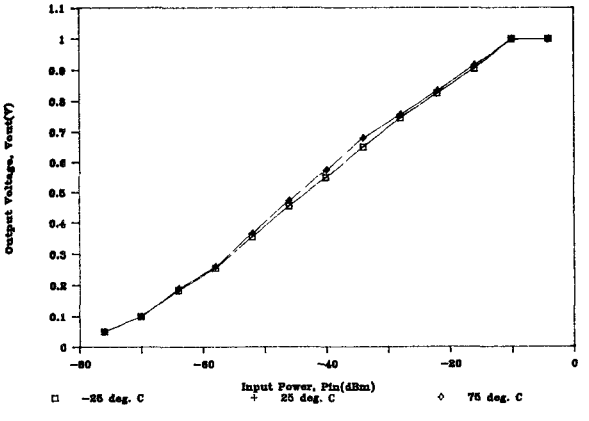

Figure 6. SDLA Transfer Curve at -25°C, 25°C and 75°C

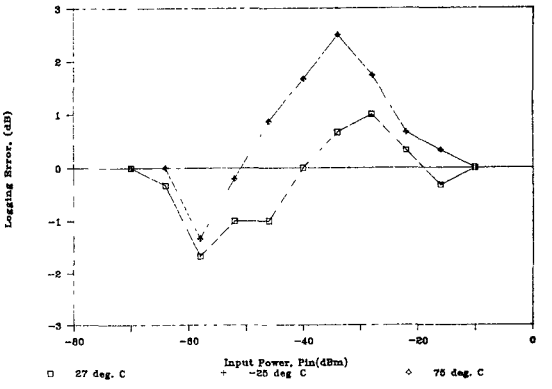

Figure 7. SDLA Error Curve at -25°C, 25°C and 75°C. Notice: -25°C and 75°C follow the same error curve.

Figure 8 is a photo of a 1 GHz 40dB RF input pulse superimposed on the logged detector video output pulse. Video pulse rise and fall times are less than 40nS. Later testing (photo not shown) performed with a faster input pulse, revealed a rise time less than 10nS.

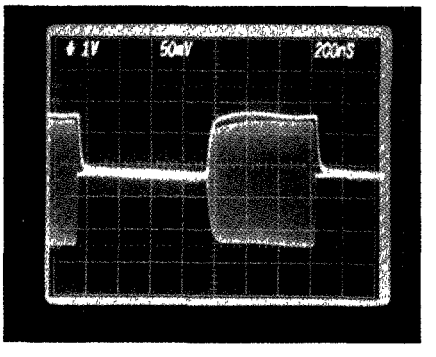

Figure 8. SDLA Pulse Response. F = 1GHz

Tangential Sensitivity (TSS) (determined through visual display) was -74dBm (4). This compared favorably with the calculated TSS (5). The following equation is utilized:

$$TSS = -114dBm + \text{Log } F_T + 10 \text{ Log } (2.5\ 2B_R B_V)$$

where -114dBm is the thermal noise floor in 1MHz of bandwidth, F_T is the noise figure of the RF amplifiers. B_R and B_V is the RF and video bandwidth, respectively. The equation yields a TSS of 74.3dBm with F_T = 8dB, B_V = 100 MHz and B_R = 700 MHz.

PACKAGING

The complete MMIC-based hybrid logarithmic amplifier was packaged into a 14 lead surface mount package measuring .38" x .38" x.08" (see Figure 9).

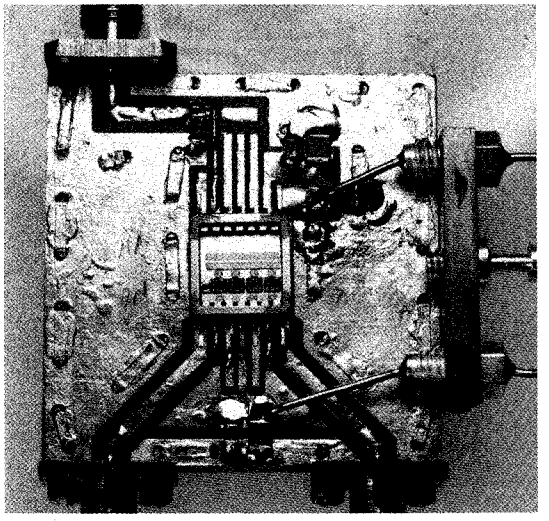

Figure 9. Complete MMIC-Based SDLA Mounted in Test Fixture

The packaging issues which warranted consideration included mounting configuration, size, electrical performance, price and reliability. The primary objective was to find a commercially available package which met the above criteria.

The package chosen is a 0.380 inch square surface mountable flat pack. It is comprised of a Kovar base and seal ring which are joined by a 7070 glass picture frame in which fourteen flat leads are supported. Once sealed with eutectic solder, the package is hermetic to less than 2.5×10^{-8} cc/sec He.

The hybrid consists of four, two-stage GaAs devices in cascade. Careful arrangement was required to eliminate possible paths for feedback. Two monolithic chip capacitors, required for bypassing, were provided for each GaAs device. The video buss, a thin film alumina substrate, collected and delivered the individual video outputs to a silicon summing amplifier. Thick film chip resistors were used in a feedback configuration for the summing amplifier and provided an RF load. Adequate space remains inside the package to accommodate a silicon voltage regulator. All components were attached to the package base with an electrically conductive, silver filled epoxy. Conventional thermosonic wedge bonding techniques were employed using 0.008 inch diameter gold wire.

CONCLUSION

An ultra-low power L-band MMIC successive detection log amplifier has been presented, packaged in a volume of only .03125 cubic inches. Excellent logging linearity, pulse response and temperature stability has been demonstrated. Next generation radar warning receivers demand channelization which, in turn, make MMIC SDLAs mandatory to meet package constraints.

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